ABSTRACT OF THE DISCLOSURE

An apparatus, method and computer program product are provided for performing a sequence of verification tests to perform hardware and software co-verification on a system under verification. The apparatus comprises a plurality of signal interface controllers operable to be coupled to the system under verification, with each signal interface controller being operable to perform one or more test actions transferring at least one of one or more stimulus signals and one or more response signals between a corresponding portion of the system under verification and the signal interface controller during performance of the sequence of verification tests. A debugger is also provided which is operable to control operation of a processing unit associated with the system under verification, the processing unit being operable to execute software routines. A debugger signal interface controller is arranged to interface with the debugger and to perform one or more test actions transferring at least one of one or more stimulus signals and one or more response signals between the debugger and the debugger signal interface controller during performance of the sequence of verification tests. A test manager coupled to the plurality of signal interface controllers and the debugger signal interface controller is operable to transfer test controlling messages to these interface controllers identifying the test actions to be performed. By this approach, the test manager is operable to control the operation of the processing unit via the debugger signal interface controller and the debugger in order to co-ordinate the execution of the software routines with a sequence of verification tests. This has been found to be a particularly efficient technique for performing hardware and software co-verification.

Fig. 3